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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/238,262	01/27/1999	JOERG SCHAEFER	10191/955	6538

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26646 7590 09/02/2003

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EXAMINER
ALANKO, ANITA KAREN

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 09/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/238,262	SCHAEFER ET AL.	
	Examiner	Art Unit	
	Anita K Alanko	1765	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/10/03 amdt "g"* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-18 and 20-24* is/are rejected.

7)☒ Claim(s) *19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14-18, 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Burns et al (U.S. Patent No. 5,738,757) and Perng (U.S. Patent No. 6,033,997).

Burns discloses a method comprising:

- providing a wafer 10 having a surface and edge areas (Fig.1A);
- dividing the surface of the wafer into positive areas (unmasked and partially masked areas in figures), to be subsequently etched in a wet chemical second etching process, and negative areas (masked areas) including the edge areas of the wafer (since the figures show that edges are not etched);
- providing the negative areas with a first passivation layer (the combination of layers 12, 14, 16 and 18) to protect the negative areas from a subsequent wet chemical second etching process;
- providing at least one of the positive areas with a second passivation layer (the combination of layers 12 and 14 in Figure 1B) having a thickness that is less (the figure shows that the layer formed by 12,14,16 and 18 is double the thickness of layer formed by 12 and 14) than a thickness of the first passivation layer;

- selectively removing the second passivation layer via a first etching process (Fig. 1D), the first etching process being terminated when the second passivation layer is completely removed;
- subsequently etching the wafer via the second wet chemical etching process (col.5, line 8) to form various openings including caverns and through-holes (Fig.1I); and
- removing the first passivation layer (Fig.1J).

Burns does not disclose providing the edge areas with a passivation layer. Perng teaches that during the processing and etching of a wafer, to protect the edges with a passivation layer 210, 270 (col.4, line 65-col.5, line 7). The layer that protects the edges is there throughout the processing to form the final product (Fig.1), which inherently requires etching steps. Therefore, it would have been obvious to one with ordinary skill in the art to provide the edge areas with a passivation layer in the method of Burns because Perng teaches that this provides additional protection at the bead region and sides of the wafer during etching of a silicon wafer.

As to claim 15, Burns discloses to apply a nitride layer 18, and to structure the nitride layer by photolithography (col.5, lines 31-32), which encompasses using a photoresist technique. The nitride layer 18 defines a part of the surface of the wafer.

As to claim 16, Burns discloses to remove the nitride layer in subareas (where 18 is not present in Figure 1B) after the first passivation layer is provided and before the wafer is etched.

As to claims 17-18, it would have been obvious to remove photoresist after exposing and developing because it is not useful during subsequent processing of the substrate.

As to claim 20, Burns discloses that the first and second passivation layers comprise oxide.

As to claims 21-24, Burns discloses to form through hole, cavern areas and a wafer of silicon (Fig.1J).

Claims 14-18, 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pearce (U.S. Patent No. 5,711,891).

Pearce discloses a method comprising:

- providing a wafer 111 having a surface and edge areas (Fig.2);
- dividing the surface of the wafer into positive areas (unmasked and partially masked areas in figures), to be subsequently etched in a wet chemical etching process, and negative areas (masked areas) including the edge areas of the wafer (since the figures show that edges are not etched; note that edge is not clearly defined and encompasses the edge of the figure depicted in Figure 2);
- providing the negative areas with a first passivation layer 131 to protect the negative areas from a subsequent wet chemical second etching process;
- providing at least one of the positive areas with a second passivation layer 132 having a thickness that is less (the figure depicts the relative thicknesses of 131 and 132) than a thickness of the first passivation layer;
- selectively removing the second passivation layer via a first process (the stripping process to remove 132; col.1, lines 52-53), the first process being terminated when the second passivation layer is completely removed;
- subsequently etching the wafer in the wet chemical second etching process (Figures 2 and 3) to form various openings including caverns and through-holes; and

- removing the first passivation layer (Figure 1 shows that the final product uses the substrate with passivation layers removed).

As to claim 14, Pearce does not explicitly disclose that the stripping process is an etching process. Examiner takes official notice that stripping processes are conventionally etching processes. Therefore, it would have been obvious to one with ordinary skill in the art to use etching for the stripping process in the method of Pearce because it is conventional in the art.

As to claims 15-18, Pearce discloses to pattern the nitride layer 133 in order to form the through-hole, but Pearce does not explicitly disclose to use a photoresist technique. It would have been obvious to one with ordinary skill to use a photoresist technique and to remove the photoresist after exposing and developing in the method of Pearce because it is a conventional technique for patterning nitride layers.

As to claim 20, Pearce discloses that the oxide layer is a thermal oxide.

Allowable Subject Matter

Claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant's point is well taken that there is no motivation to perform a LOCOS process to form a planar layer as disclosed by Burns. LOCOS is a local oxidation step to form a patterned layer, not oxidation to form a blanket layer. There is also no motivation to perform a LOCOS process in the method of Pearce because Pearce suggests to pattern a thermal oxide,

such as shown in Figure 5, rather than form a patterned thick oxide layer through an oxidation mask.

Claim Construction

Examiner interprets the term "edge areas" to comprise the areas on the side of the wafer that are in between the top (planar) surface and the bottom (planar) surface. It does not encompass a region on either the top surface or the bottom surface. Any other intended significance of the term "edge areas" must be explicitly recited by applicant.

Examiner interprets "LOCOS" process to comprise forming a silicon nitride mask, thermal oxidation of silicon through said mask to form the silicon oxide, and stripping of the nitride mask. The term describes a conventional technique in the art, as for example, discussed by Takiyama et al (US 5,762,813) at column 1, lines 15-26.

Response to Amendment

Claims 14-18, 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Burns et al (U.S. Patent No. 5,738,757) and Perng (U.S. Patent No. 6,033,997).

Claims 14-18, 20-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pearce (U.S. Patent No. 5,711,891).

Claim 19 is objected to, but would be allowable in independent form.

Response to Arguments

As to claims 14-18 and 20-24, applicant's arguments filed 07/10/2003 are not persuasive. Applicant's arguments are not commensurate in scope with the claim language. The claims do not cite forming a first passivation layer directly on the wafer selectively only on the negative areas. The claims do not cite that the passivation layers are deposited only on the negative or positive areas, they only cite that they "include" those areas. The figures show the relative order of the etching steps cited. Note also that Pearce discloses that oxide layer seals the edges of the wafer (col.3, lines 15-20), which encompasses the claimed passivation step.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anita K Alanko whose telephone number is 703-305-7708. The examiner can normally be reached on Monday-Wednesday and Friday, 8:00 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 703-305-2667. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

Anita K. Alanko

Anita K Alanko
Primary Examiner
Art Unit 1765

AKA
August 22, 2003